Amendments to the Specification:

Please replace paragraph beginning on page 16, line 10 with the following amended paragraph:

Figure 3 shows a cellular switching system 410. The system 410 has one or more Mobile Stations (MS) 412 that can transmit and receive data on-demand using a plurality of channels bonded together. The system 410 also has a Base Station Subsystem (BSS) 414, a Network and Switching Subsystem (NSS) 416, and an Operation and Support Subsystem (OSS), not shown. The BSS 414 connects the MS 412 and the NSS and is in charge of the transmission and reception. The BSS 414 includes a Base Transceiver Station (BTS) or Base Station 420 and a Base Station Controller (BSC) 422.

Please replace paragraph beginning on page 9, line 1 with the following amended paragraph:

In one exemplary sequence in the embodiment of FIG. 1A, the mobile station requests two channels, and in this example, channels 1 and 2 in FIG. 1B at ~~890.0~~ 890.2 MHz and 890.4 MHz are available. The base station responds by sending the ~~890.0~~ 890.2 and 890.4 MHz frequency identification to the mobile station. The mobile station in turn updates its transceiver with the frequency information, and the transceiver can listen for data in all frames associated with the 890.2 and 890.4 MHz channels. In this example, two frequency channels have been bonded together to increase transmission bandwidth.

Please replace paragraph beginning on page 10, line 3 with the following amended paragraph:

The reconfigurable processor core 150 can include one or more processors 151 such as MIPS processors and/or one or more digital signal processor (DSPs) 153, among others. The reconfigurable processor core 150 has a bank of efficient processors 151 and a bank of DSPs 153 with embedded functions. These processors 151 and 153 can be configured to operate optimally on specific problems and can include buffers on the receiving end and buffers on the transmitting end ~~such the buffers shown in FIG. 1~~. For example, the bank of DSPs 153 can be optimized to handle discrete cosine transforms (DCTs) or Viterbi encodings, among others. Additionally, dedicated hardware 155 can be provided to handle specific algorithms in silicon more efficiently than programmable processors 151 and 153. The number of active processors is controlled depending on the application, so that power is not used when it is not needed. This embodiment

does not rely on complex clock control methods to conserve power, since the individual clocks are not run at high speed, but rather the unused processor is simply turned off when not needed.